

*Sub*  
*CO*  
performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; and

*Contd*  
*B1*  
performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature, the first and second post-annealings being performed after the forming of the plate electrode.

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